AMENDMENT UNDER 37 C.F.R. § 1.114
Application No.: 09/347,409
Attorney Docket No. Q55026

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-3. (Canceled).

4. (Currently Amended) A method of calculating, by the use of a computer, pin-to-pin delay time T_{iopath_aged}, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between ~~said~~ two said logic blocks connected to each other, comprising:

(a) calculating an amount of stress S_{in} cast by the input pin and an amount of stress S_{out} cast by the output pin according to the following expression:

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by α and β, and width of channel of ~~the~~ a transistor connected to ~~the~~ a pin is represented by W [μm];

(b) calculating an aged delay time of the input pin δ_{in} [%] and an aged delay time of the output pin δ_{out} [%] according to the following expression:

$$\delta = \gamma \left(\frac{\tau S f}{\varepsilon_1 e^{\kappa T}} \right)^{\frac{1}{\varepsilon_2}}$$

where a constant depending on physical structure of the pin is represented by γ, the term of guarantee of ~~the~~ a LSI is represented by τ [hour], constants depending on process are represented by $\varepsilon 1$, $\varepsilon 2$ and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating and outputting for use as values representative of circuit properties of ~~said~~ a logic level circuit the pin-to-pin delay time T_{iopath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_aged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

where pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by T_{iopath_fresh} [ps] and $T_{connect\_fresh}$ [ps], and ratios of delay times occurred at ~~the~~ an input stage and ~~the~~ an output stage to whole delay time occurred from the input pin to the output pin are represented by λ_{in} and λ_{out}.

5. (Canceled).

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6. (Currently Amended): A method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, comprising:

(a) calculating ~~delay times of all said logic blocks according~~ pin-to-pin delay time T_{iopath_aged}, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between two said logic blocks connected to each other, comprising:

(i) calculating an amount of stress S_{in} cast by the input pin and an amount of stress S_{out} cast by the output pin according to the following expression:

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by α and β, and width of channel of a transistor connected to a pin is represented by W [μm];

(ii) calculating an aged delay time of the input pin δ_{in} [%] and an aged delay time of the output pin δ_{out} [%] according to the following expression:

$$\delta = \gamma\left(\frac{\tau Sf}{\varepsilon_1 e^{\kappa T}}\right)^{\frac{1}{\varepsilon_2}}$$

where a constant depending on physical structure of the pin is represented by γ, the term of guarantee of a LSI is represented by τ [hour], constants depending on process are represented by $\varepsilon 1$, $\varepsilon 2$ and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(iii) calculating and outputting for use as values representative of circuit properties of the logic level circuit the pin-to-pin delay time T_{iopath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_oged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

where pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by T_{iopath_fresh} [ps] and $T_{connect\_fresh}$ [ps], and ratios of delay times occurred at an input stage and an output stage to whole delay time occurred from the input pin to the output pin are represented by λ_{in} and λ_{out} ~~to the method as in claim 4~~; and

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

7-9. (Canceled).

10. (Currently Amended) A computer-readable medium incorporating a program of instructions for calculating, by using a computer, pin-to-pin delay time T_{iopath_aged}, which is delay

time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between ~~said~~ two said logic blocks connected to each other, the program making a computer execute the following processes:

(a) calculating an amount of stress S_{in} cast by the input pin and an amount of stress S_{out} cast by the output pin according to the following expression:

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by α and β, and width of channel of ~~the~~ a transistor connected to ~~the~~ a pin is represented by W [μm];

(b) calculating an aged delay time of the input pin δ_{in} [%] and an aged delay time of the output pin δ_{out} [%] according to the following expression:

$$\delta = \gamma\left(\frac{\tau Sf}{\varepsilon_1 e^{\kappa T}}\right)^{\frac{1}{\varepsilon_2}}$$

where that a constant depending on physical structure of the pin is represented by γ, the term of a guarantee of ~~the~~ a LSI is represented by τ [hour], constants depending on process are represented by ε1, ε2 and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(c) calculating and outputting for use as values representative of circuit properties of ~~said~~ a logic level circuit the pin-to-pin delay time T_{iopath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_aged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

where pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by T_{iopath_fresh} [ps] and $T_{connect\_fresh}$ [ps], and ratios of delay times occurred at ~~the~~ an input stage and ~~the~~ an output stage to whole delay time occurred from the input pin to the output pin are represented by λ_{in} and λ_{out}, respectively.

11. (Canceled).

12. (Currently Amended): A computer-readable medium incorporating a program of instructions for calculating a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks, the program making a computer execute the following processes:

(a) calculating pin-to-pin delay time T_{iopath_aged}, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time $T_{connect\_aged}$, which is delay time of a signal passing between two said logic blocks connected to each other, said calculating comprises:

(i) calculating an amount of stress S_{in} cast by the input pin and an amount of stress S_{out} cast by the output pin according to the following expression:

$$S = \alpha\left(\frac{C}{W}\right)^{\beta}$$

where a load capacitance is represented by C [pF], constants depending on change of inputted waveform are represented by α and β, and width of channel of a transistor connected to a pin is represented by W [μm];

(ii) calculating an aged delay time of the input pin δ_{in} [%] and an aged delay time of the output pin δ_{out} [%] according to the following expression:

$$\delta = \gamma\left(\frac{\tau S f}{\varepsilon_1 e^{\kappa T}}\right)^{\frac{1}{\varepsilon_2}}$$

where that a constant depending on physical structure of the pin is represented by γ, the term of a guarantee of a LSI is represented by τ [hour], constants depending on process are represented by $\varepsilon 1$, $\varepsilon 2$ and κ, working frequency is represented by f [Hz], and absolute temperature is represented by T [K];

(iii) calculating and outputting for use as values representative of circuit properties of said logic level circuit the pin-to-pin delay time T_{ipath_aged} and the block-to-block delay time $T_{connect\_aged}$ according to the following expressions:

$$T_{iopath\_aged} = T_{iopath\_fresh}\left(1 + \lambda_{in}\delta_{in} + \lambda_{out}\delta_{out}\right)$$
$$T_{connect\_aged} = T_{connect\_fresh}\left(1 + \lambda_{out}\delta_{out}\right)$$

where pin-to-pin delay time and block-to-block delay time calculated ignoring aging caused by hot carrier effect are represented by T_{iopath_fresh} [ps] and $T_{connect\_fresh}$ [ps], and ratios of delay times occurred at an input stage and an output stage to whole delay time occurred from the input pin to the output pin are represented by λ_{in} and λ_{out}, respectively~~calculating delay times of all said logic blocks according to the program as in claim 10~~; and~~,~~

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a).

13-16. (Canceled).